WHAT IS CLAIMED IS:

1. A modulation apparatus using a mixed-radix fast Fourier transform (FFT), comprising:

an input/output interface for selecting a memory for input/output among memories for input/output and FFT calculation, selecting one of four banks of the selected memory, and performing input and output on the selected bank;

two N-word memories each having four banks used for input/output to the input/output interface and FFT calculation;

a first data exchange for selecting a memory for FFT calculation among the memories for input/output to the input/output interface and FFT calculation, and connecting banks assigned to each butterfly input/output to 4 inputs of a butterfly calculation circuit for in-place calculation;

a butterfly for performing a radix-4 butterfly and a radix-2 butterfly provided from the first data exchange with one circuit, and forming a symmetric reverse output;

a second data exchange for selecting a memory for FFT calculation among the memories for input/output to the input/output interface and FFT calculation, and connecting banks assigned to each butterfly input/output to four outputs of a butterfly calculation circuit for in-place calculation; and

an address generator for generating a bank index and an address for performing in-place calculation in a multi-bank memory structure.

2. The modulation apparatus of claim 1, wherein the butterfly is a radix-4/2 butterfly calculation circuit capable of simultaneously performing sequential input and output by forming a symmetric reverse output sequence by exchanging outputs of a radix-4 butterfly and two radix-2 butterflies, so that continuous processing can be performed with the two N-word memories each including four banks.

3. The modulation apparatus of claim 1, wherein the in-place algorithm is determined by modifying an in-place algorithm of a radix-4 algorithm-based multi-bank memory structure.

4. The modulation apparatus of claim 1, wherein the in-place algorithm separately includes an $(n-2)^{th}$ bit in modulo-4 addition during 2^n-point calculation in generating a bank index.

5. A modulation apparatus using a mixed-radix fast Fourier transform (FFT), comprising:

two memories each having four banks, for writing input symbols or FFT-calculated symbols;

a butterfly for performing butterfly calculation in a radix-4 mode or a radix-2 mode according to the number of symbols output from the memories, and outputting the calculated values in a symmetric reverse;

a first data exchange for reading one symbol from each bank of one of the memories and outputting the read symbol to the butterfly;

a second data exchange for matching calculated symbols output from the butterfly so that the symbols are written in the same addresses as addresses where the symbols were read from the first data exchange; and

an address generator for controlling an output of the second data exchange so that when a symbol read from the first data exchange is output through the second data exchange after being calculated, a bank and an address where the symbol was read from the first data exchange are identical to an output bank and an output address of the second data exchange.

6. The modulation apparatus of claim 5, further comprising an input/output interface for performing interfacing between input/output data and the two memories.

7. The modulation apparatus of claim 5, wherein the butterfly has a radix-4 butterfly structure and is designed so that when radix-2 calculation is required, two radix-2 calculations are performed through a multiplexer included in the butterfly.

8. The modulation apparatus of claim 5, wherein for symmetric reverse of the butterfly, a binary output count value determined by the total number of symbols being subject to the butterfly calculation is symmetrically converted into an address by the 2 bits.

9. The modulation apparatus of claim 8, wherein when a digit of the binary output count value is an odd number, an address is determined by performing symmetrical conversion on the basis of a center bit of the digit.

10. The modulation apparatus of claim 5, wherein the address generator determines a bank with a value determined by performing modulo-4 calculation on a binary input count bit value corresponding to the calculated symbol.

11. The modulation apparatus of claim 10, wherein the address generator, when a digit of the binary input count bit is an odd number, determines a bank by exchanging positions of two most significant bits, performing modulo-4 calculation by the low two bits, and then performing modulo-4 calculation on the position-exchanged most significant bits.